```
--------------------------------------------------------------------------------
Xilinx TRACE, Version D.19
Copyright (c) 1995-2000 Xilinx, Inc.  All rights reserved.

trce lab3b-.ncd lab3b-.pcf -e 3 -o lab3b-.twr

Design file:              lab3b-.ncd
Physical constraint file: lab3b-.pcf
Device,speed:             xc4010xl,-09 (C 1.1.2.2 PRELIMINARY)
Report level:             error report
--------------------------------------------------------------------------------

WARNING:Timing:2491 - No timing constraints found, doing default enumeration.

================================================================================
Timing constraint: Default period analysis
 2116 items analyzed, 0 timing errors detected.
 Minimum period is  24.950ns.
--------------------------------------------------------------------------------

================================================================================
Timing constraint: Default net enumeration
 79 items analyzed, 0 timing errors detected.
 Maximum net delay is   6.500ns.
--------------------------------------------------------------------------------


All constraints were met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock $Net00066_
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
$Net00004_     |    2.103(R)|    1.288(R)|
$Net00005_     |    3.369(R)|    1.097(R)|
$Net00006_     |    3.846(R)|    0.281(R)|
$Net00007_     |    3.693(R)|    0.802(R)|
$Net00008_     |   -2.281(R)|    3.151(R)|
---------------+------------+------------+

Clock $Net00066_ to Pad
---------------+------------+
               | clk (edge) |
Destination Pad|   to PAD   |
---------------+------------+
S0             |   22.523(R)|
S1             |   23.029(R)|
S2             |   22.828(R)|
S3             |   23.290(R)|
S4             |   23.161(R)|
S5             |   23.854(R)|
S6             |   22.951(R)|
---------------+------------+

Clock to Setup on destination clock $Net00066_
---------------+---------+---------+---------+---------+
               | Src/Dest| Src/Dest| Src/Dest| Src/Dest|
Source Clock   |Rise/Rise|Fall/Rise|Rise/Fall|Fall/Fall|
---------------+---------+---------+---------+---------+
$Net00066_     |   24.950|         |         |         |
---------------+---------+---------+---------+---------+


Timing summary:
---------------

Timing errors: 0  Score: 0
```

Constraints cover 2116 paths, 79 nets, and 266 connections (100.0% coverage)

Design statistics:
   Minimum period: 24.950ns (Maximum frequency: 40.080MHz)
   Maximum net delay: 6.500ns

WARNING:Timing - Clock nets using non-dedicated resources were found in this
   design. Clock skew on these resources will not be automatically addressed
   during path analysis. To create a timing report that analyzes clock skew for
   these paths, run trce with the '-skew' option.

   The following clock nets use non-dedicated resources:
      CLK

Analysis completed Wed Jun 19 14:53:03 2002
