

```

1: library IEEE;
2: use IEEE.std_logic_1164.all;
3:
4: entity control_logic is
5: port (
6:   clock: in STD_LOGIC;
7:   reset: in STD_LOGIC;
8:   scounter: in STD_LOGIC_VECTOR(2 downto 0);
9:   instruction: in STD_LOGIC_VECTOR(7 downto 0);
10:  r0_bus: out STD_LOGIC;
11:  r1_bus: out STD_LOGIC;
12:  ld_out: out STD_LOGIC;
13:  lsl_r0: out STD_LOGIC;
14:  lsl_r1: out STD_LOGIC;
15:  swap_r0_r1: out STD_LOGIC;
16:  ld_r0: out STD_LOGIC;
17:  ld_r1: out STD_LOGIC;
18:  clr_r0: out STD_LOGIC;
19:  clr_r1: out STD_LOGIC;
20:  clr_temp: out STD_LOGIC;
21:  clr_out: out STD_LOGIC;
22:  ld_temp: out STD_LOGIC;
23:  clr_mbr: out STD_LOGIC;
24:  clr_mar1: out STD_LOGIC;
25:  ld_mar1: out STD_LOGIC;
26:  ld_mbr: out STD_LOGIC;
27:  clr_pc: out STD_LOGIC;
28:  clr_ir: out STD_LOGIC;
29:  ld_pc: out STD_LOGIC;
30:  ld_ir: out STD_LOGIC;
31:  clr_scntr: out STD_LOGIC;
32:  ceb: out STD_LOGIC;
33:  oeb: out STD_LOGIC;
34:  web: out STD_LOGIC;
35:  temp_bus: out STD_LOGIC
36: );
37: end control_logic;
38:
39: architecture control_logic_arch of control_logic is
40: begin
41:   process(instruction, clock, scounter)
42:     begin
43:       if(clock'event and clock = '1') then
44:         case instruction(7 downto 4) is
45:
46:           -- R0 > OUT
47:           when "0000" => if(scounter="000") then
48:             r0_bus <= '1';
49:             ld_out <= '1';
50:             clr_scntr <= '1';
51:             end if;
52:
53:           -- R1 > OUT
54:           when "0001" => if(scounter="000") then
55:             r1_bus <= '1';
56:             ld_out <= '1';
57:             clr_scntr <= '1';
58:             end if;
59:
60:           -- RO < LSL R0

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61:           when "0010" =>      if(scounter="000") then
62:                           lsl_r0 <= '1';
63:                           clr_scntr <= '1';
64:                           end if;
65:
66:           -- R1 < LSL R1
67:           when "0011" =>      if(scounter="000") then
68:                           lsl_r1 <= '1';
69:                           clr_scntr <= '1';
70:                           end if;
71:
72:           -- R0 > TMP ; R1 > R0 ; TMP > R1
73:           when "0100" =>      if(scounter="000") then
74:                           swap_r0_r1 <= '1';
75:                           r0_bus <= '1';
76:                           ld_temp <= '1';
77:                           r1_bus <= '1';
78:                           ld_r0 <= '1';
79:                           temp_bus <= '1';
80:                           ld_r1 <= '1';
81:                           clr_scntr <= '1';
82:                           end if;
83:           -- R0 < MEM
84:           when "0101" =>      if(scounter="000") then
85:                           ld_r0 <= '1';
86:                           ceb <= '0';
87:                           oeb <= '0';
88:                           web <= '1';
89:                           end if;
90:
91:           -- R1 < MEM
92:           when "0110" =>      if(scounter="000") then
93:                           ld_r1 <= '1';
94:                           ceb <= '0';
95:                           oeb <= '0';
96:                           web <= '1';
97:                           end if;
98:
99:           -- MEM < R0
100:          when "0111" =>      if(scounter="000") then
101:                          r0_bus <= '1';
102:                          ceb <= '0';
103:                          oeb <= '1';
104:                          web <= '0';
105:                          end if;
106:
107:          -- MEM < R1
108:          when "1000" => if(scounter="000") then
109:                          r1_bus <= '1';
110:                          ceb <= '0';
111:                          oeb <= '1';
112:                          web <= '0';
113:                          end if;
114:
115:          when others => null;
116:      end case;
117:  end if;
118: end process;
119: end control_logic_arch;

```